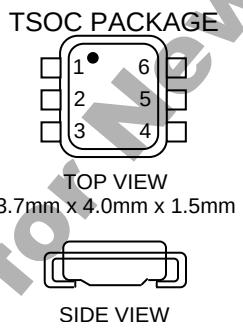
# DS2423
## 4kbit 1-Wire RAM with Counter



## FEATURES
- 4096 bits of SRAM
- Four 32-bit, read-only counters
- Active-low external trigger inputs for two of the counters with on-chip debouncing compatible with reed and Wiegand switches
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Memory partitioned into 16 256-bit pages in for packetizing data
- 256-bit scratchpad with strict read/write protocols ensures integrity of data transfer
- On-chip 16-bit CRC generator for safeguarding data transfers
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits per second
- Overdrive mode boosts communication speed to 142kbits per second
- 8-bit family code specifies device communication requirements to reader
- Presence detector acknowledges when reader first applies voltage
- Compact, low cost 6-pin TSOC surface mount package
- Reads, writes and counts over a wide voltage range of 2.8V to 5.5V from -40°C to +85°C

## PIN ASSIGNMENT




## PIN DESCRIPTION

| | |
|---|---|
| Pin 1 | Ground |
| Pin 2 | Data |
| Pin 3 | Vbat |
| Pin 4 | NC |
| Pin 5 | Input channel B |
| Pin 6 | Input channel A |

## ORDERING INFORMATION

| | |
|---|---|
| DS2423P | 6-pin TSOC package |
| DS2423P/T&R | Tape & Reel Version of DS2423P |
| DS2423P+ | 6-pin TSOC package |

*+ Indicates lead-free compliance.*

## DESCRIPTION

The DS2423 1-Wire® RAM with Counters is a fully static, read/write memory for battery operation in a low-cost, six-lead TSOC, surface-mount package. The memory is organized as 16 pages of 256 bits each. In addition, the device has four counters, two of them with external trigger inputs called A and B. Each of the counters is associated with a memory page. A counter without external trigger input increments each time data is written to the page it is associated with (write cycle counter). The counters triggered by inputs A and B, respectively, increment with every low-going pulse on their input. All counters are read-only. They are automatically cleared to 0 when the battery is connected.

The battery-backed memory offers a simple solution to storing and retrieving information pertaining to the equipment where the DS2423 is installed and its frequency of use. The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it may be read back for verification. A copy scratchpad command will then transfer the data to memory. This process ensures data integrity when modifying the memory. A 64-bit registration number is factory lasered into each DS2423 to provide a guaranteed unique identity which allows for absolute traceability and acts as node address if multiple DS2423 are connected in parallel to form a local network. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return.

The DS2423 1-Wire RAM with Counters can store encrypted data. The unique registration number and the page write cycle counter(s) prevent unauthorized manipulation of data stored in a page with a write cycle counter associated.



## OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2423. The DS2423 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) four 32-bit read-only counters. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. Each of these counters is associated with one of the 256-bit memory pages. The four counters of the DS2423 are associated with pages 12 to 15. The contents of the counter are read together with the memory data using a special command. The bus master must first provide one of the six ROM Function Commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the five memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

## PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry steals power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved, and 2) if the battery is exhausted for any reason, the ROM may still be read normally.

## 64-BIT LASERED ROM

Each DS2423 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits (See Figure 3). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in Application Note 27. The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the $8^{th}$ bit of the family code has been entered, then the serial number is entered. After the $48^{th}$ bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | -0.5V to +7.0V |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -55°C to +125°C |
| Soldering Temperature | See J-STD-020A Specifications |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## DC CHARACTERISTICS ($V_{PUP}$ = 2.8V to 6.0V; $V_{BAT}$ = 2.8 to 5.5V;-40°C to +85°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.2 | | | V | 1, 8 |
| Logic 0 | $V_{IL}$ | -0.3 | | +0.8 | V | 1, 9 |
| Output Logic Low @ 4 mA | $V_{OL}$ | | | 0.4 | V | 1 |
| Output Logic High | $V_{OH}$ | | $V_{PUP}$ | 6.0 | V | 1, 2 |
| Input Load Current | $I_L$ | | 5 | | µA | 3 |
| Standby Current | $I_{BATS}$ | | | 200 | nA | |
| I/O Operate Charge | $Q_{BATO}$ | | | 200 | nC | 12, 16 |

## CAPACITANCE

($t_A$ = 25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| I/O (1-Wire) | $C_{IN/OUT}$ | | 100 | 800 | pF | 6, 16 |

## COUNTER INPUT CHARACTERISTICS

($V_{PUP}$ = 2.8V to 6.0V; $V_{BAT}$ = 2.8 to 5.5V;-40°C to +85°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Trip Point | $V_{TRIP}$ | | ½ $V_{BAT}$ | | V | |
| Logic 1 | $V_{INH}$ | $V_{TRIP}$ | | $V_{BAT}$ +0.3 | V | 1, 10 |
| Logic 0 | $V_{INL}$ | -0.3 | | $V_{TRIP}$ | V | 1 |
| Internal Pullup Resistor | $R_{PI}$ | | 28 | | Mς | 11, 16 |
| Debounce Time | $T_{DEB}$ | 170 | 290 | 460 | µs | 13 |
| Pulse Width (Active Low) | $T_{PW}$ | 1 | | | µs | 16 |

## AC CHARACTERISTICS REGULAR SPEED

($V_{PUP}$ = 2.8V to 6.0V; $V_{BAT}$ = 2.8 to 5.5V;-40°C to +85°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Time Slot | $t_{SLOT}$ | 60 | | 120 | µs | |
| Write 1 Low Time | $t_{LOW1}$ | 1 | | 15 | µs | 15 |
| Write 0 Low Time | $t_{LOW0}$ | 60 | | 120 | µs | |
| Read Low Time | $t_{LOWR}$ | 1 | | 15 | µs | 15 |
| Read Data Valid | $t_{RDV}$ | | 15 | | µs | 14, 16 |
| Release Time | $t_{RELEASE}$ | 0 | 15 | 45 | µs | |
| Read Data Setup | $t_{SU}$ | | | 1 | µs | 5 |
| Recovery Time | $t_{REC}$ | 1 | | | µs | |
| Reset Time High | $t_{RSTH}$ | 480 | | | µs | 4 |
| Reset Time Low | $t_{RSTL}$ | 480 | | 960 | µs | 7 |
| Presence Detect High | $t_{PDH}$ | 15 | | 60 | µs | |
| Presence Detect Low | $t_{PDL}$ | 60 | | 240 | µs | |

## AC CHARACTERISTICS OVERDRIVE SPEED

($V_{PUP}$ = 2.8V to 6.0V; $V_{BAT}$ = 2.8 to 5.5V;-40°C to +85°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Time Slot | $t_{SLOT}$ | 6 | | 16 | µs | |
| Write 1 Low Time | $t_{LOW1}$ | 1 | | 2 | µs | 15 |
| Write 0 Low Time | $t_{LOW0}$ | 6 | | 16 | µs | |
| Read Low Time | $t_{LOWR}$ | 1 | | 2 | µs | 15 |
| Read Data Valid | $t_{RDV}$ | | 2 | | µs | 14, 16 |
| Release Time | $t_{RELEASE}$ | 0 | 1.5 | 4 | µs | |
| Read Data Setup | $t_{SU}$ | | | 1 | µs | 5 |
| Recovery Time | $t_{REC}$ | 1 | | | µs | |
| Reset Time High | $t_{RSTH}$ | 48 | | | µs | 4 |
| Reset Time Low | $t_{RSTL}$ | 48 | | 80 | µs | |
| Presence Detect High | $t_{PDH}$ | 2 | | 6 | µs | |
| Presence Detect Low | $t_{PDL}$ | 8 | | 24 | µs | |

## NOTES:

1) All voltages are referenced to ground.

2) $V_{PUP}$ = external pullup voltage.

3) Input load is to ground.

4) An additional reset or communication sequence cannot begin until the reset high time has expired.

5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge.

6) Capacitance on the data pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to $V_{PUP}$, 5µs after power has been applied the parasite capacitance will not affect normal communications.

7) The reset low time ($t_{RSTL}$) should be restricted to a maximum of 960µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

8) $V_{IH}$ is a function of the external pullup resistor and $V_{PUP}$.

9) Under certain low voltage conditions $V_{ILMAX}$ may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.

10) The counter inputs are designed for interfacing to mechanical switches and piezo sensors. If interfacing to digital circuits, one should use an open drain driver.

11) A lower impedance pullup, e. g., for reed switches, can be achieved by connecting an external resistor from the counter input to $V_{BAT}$.

12) Read and write scratchpad (all 32 bytes) at $V_{BAT}$ of 3.0 V.

13) Each low-going edge on a counter input resets the channel's debounce timer. The debounce time starts as the input voltage rises beyond the trip point. In order for the next pulse to be counted the debounce time must have expired.

14) The optimal sampling point for the master is as close as possible to the end time of the $t_{RDV}$ period without exceeding $t_{RDV}$. For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.

15) The duration of the low pulse sent by the master should be a minimum of 1µs with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.

16) Guaranteed by design; not production tested.